## REMARKS/ARGUMENTS

Claims 2-8, 10, 12, and 18-27 are pending in this application. By this Amendment, Applicants ADD claims 18-27.

Claims 2, 4-8, 10, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Sano (5,190,892) and Dohya (4,665,468). Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Sano and Dohya, and further in view of Kitamura et al. (5,480,048). Applicants respectfully traverse the rejections of claims 2-8, 10, and 12.

Claim 5 recites:

> "A method of producing a high frequency circuit chip having a substrate made of a ceramic with a high dielectric constant, a wiring pattern provided on one main surface of the substrate, an electric conductor layer provided on substantially all of another main surface of the substrate, and a through-hole including a connecting electrode for connecting the wiring pattern and the conductor layer to each other, the method comprising the steps of:
>
> filling electrically conductive paste into a perforation in the substrate, and firing the paste to form the connecting electrode of the through-hole;
>
> forming a resist pattern with an opening having a desired shape and size directly on the substrate;
>
> forming a thin film with a wiring material directly on the substrate through the opening over the resist pattern after forming the resist pattern;
>
> removing the unnecessary wiring material thin film deposited on the resist pattern together with the resist pattern to form the wiring pattern directly on the substrate by a lift-off method;
>
> **mirror-polishing at least the surface of the fired substrate on which the wiring pattern is formed, and the fired substrate in which the through-hole having the connecting electrode is formed**; and
>
> thereafter forming the wiring pattern on the mirror-polished surface by the lift-off method." (emphasis added)

Applicants' claim 5 recites the step of "mirror-polishing at least the surface of the fir d substrate on which the wiring pattern is formed, and the fired substrate in which the

through-hole having the connecting electrode is formed." Applicants' claim 10 recites features which are similar to features recited in Applicants' claim 5, including the above emphasized features. With the improved features of claims 5 and 10, Applicants have been able to provide a method of efficiently producing a high frequency circuit chip having a decreased size and a fine, high precision wiring pattern (see, for example, the sixth full paragraph on page 2 of the originally filed Specification).

Applicants agree with the Examiner that neither AAPA nor Sano teach or suggest the feature of "mirror-polishing at least the surface of the fired substrate on which the wiring pattern is formed, and the fired substrate in which the through-hole having the connecting electrode is formed" as recited in Applicants' claims 5 and 10. The Examiner has relied upon Dohya to allegedly cure this deficiency.

The Examiner has stated in the third paragraph on page 3 of the outstanding Office Action that it would have been obvious to modify the method of the combination of AAPA and Sano with the teachings of Dohya "in order to prevent the undulation of the surface of the substrate." However, the undulations of the substrate **10** of Dohya are caused because substrate **10** is a multilayer substrate. That is, the uneven combination of alumina substrates **11** and ground layers **12** cause the undulations in the multilayer substrate **10**. Unlike Dohya, AAPA and Sano only teach the use of a single layer substrate **1**. Thus, one of ordinary skill in the would not have modified the combined teachings of AAPA and Sano in view Dohya because Dohya is directed to solving problems associated with a multilayer substrate and AAPA and Sano are directed to a single layer substrate, which clearly would not have the problems associated with a multilayer substrate. The Examiner is reminded that Prior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings. In re. Sernaker, 217 USPQ 1 (Fed. Cir. 1983). Because Dohya does not teach or suggest anything about a single layer substrate, Dohya clearly fails to teach or suggest polishing a single layer substrate.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 5 and 10 under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Sano and Dohya.

The Examiner has relied upon Kitamura et al. to allegedly cure various deficiencies in the combination of AAPA, Sano, and Dohya. However, Kitamura et al. fails to teach or suggest the feature of "mirror-polishing at least the surface of the fired substrate on which the wiring pattern is formed, and the fired substrate in which the through-hole having the connecting electrode is formed" as recited in Applicants' claims 5 and 10.

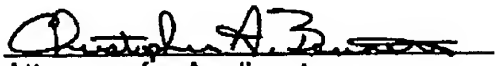
Accordingly, Applicants respectfully submit that AAPA, Sano, Dohya, and Kitamura et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 5 and 10 of the present application. Claims 2-4, 6-8, and 18-22 depend upon claim 5 and are therefore allowable for at least the reasons that claim 5 is allowable. Claims 12 and 23-27 depend upon claim 10 and are therefore allowable for at least the reasons that claim 10 is allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: January 20, 2004



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